Radionica digitalnog dizajna IV

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Centar za svemirsku i inovativnu tehnologiju

17. ožujka 2024.

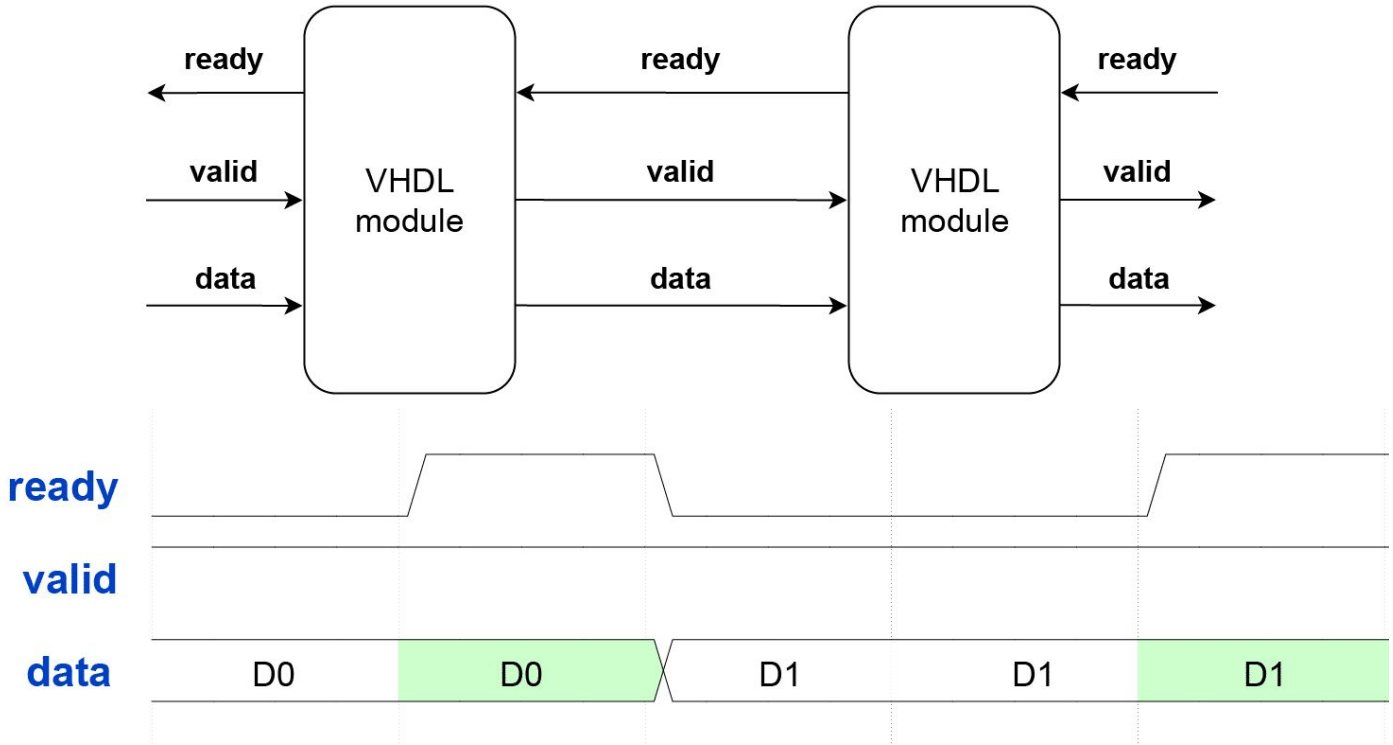
wlan: kpckat
pass:kpc123456

Raspored

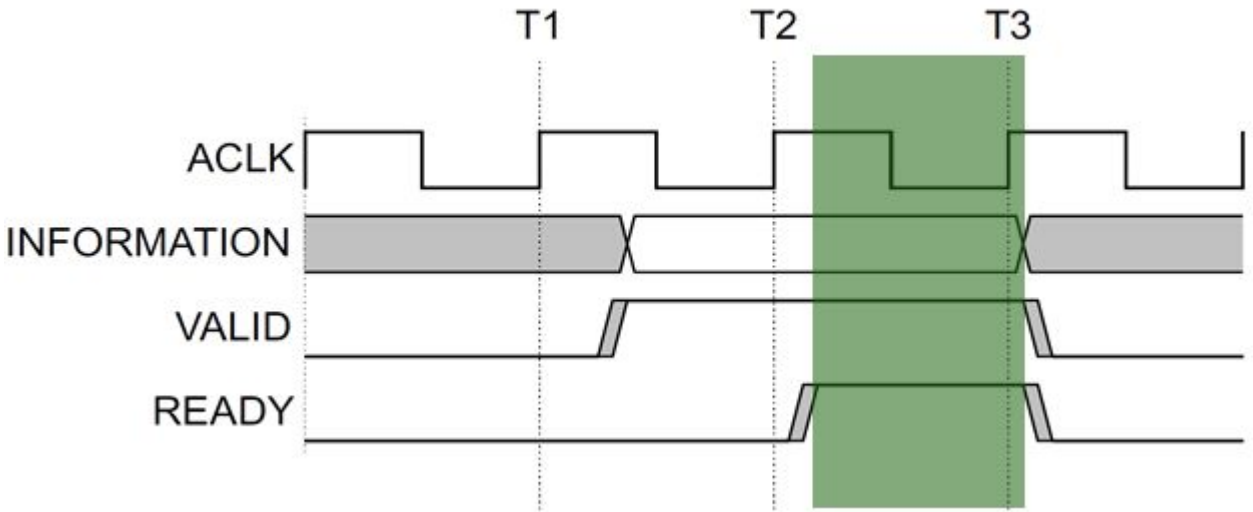
17. ožujak 2024., nedjelja	
9.00 - 12.00	● Memorijska sučelkja ● Automati ● Rad na tt06-csit-luks (I)
12.00 - 12.4	Pauza za ručak
12.45 - 15.00	● Rad na tt06-csit-luks (II)

Memorijska sučelja

VALID/READY access (I)

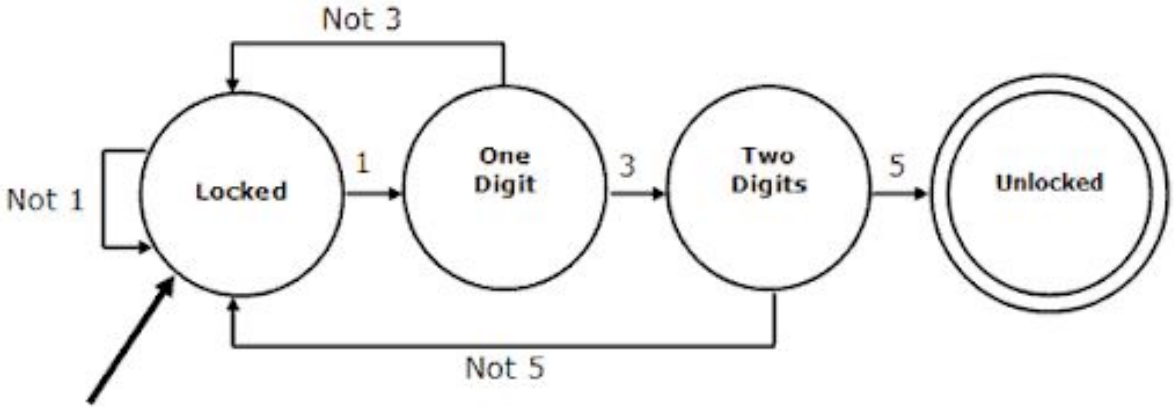


VALID/READY access (II)

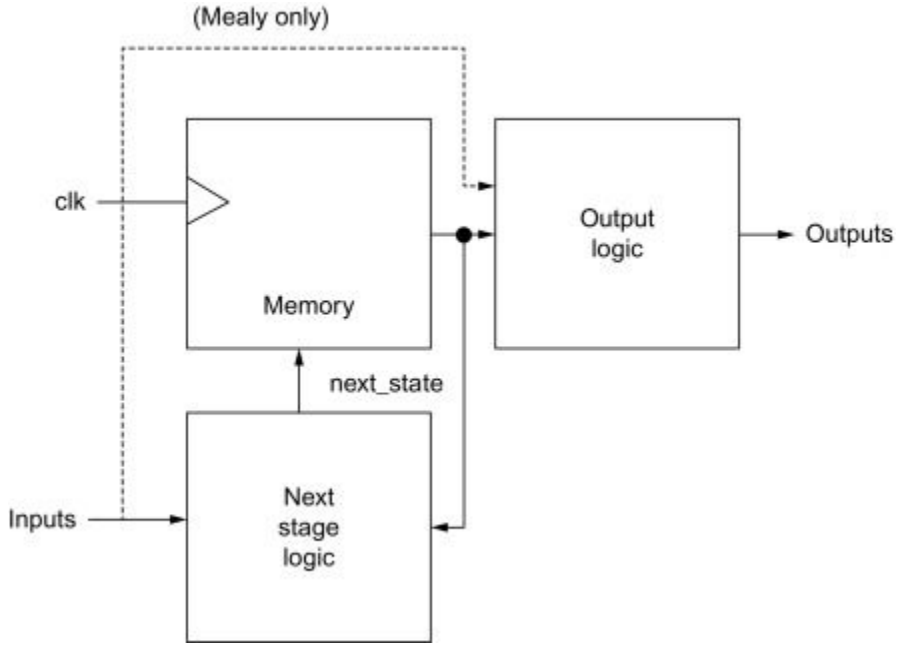


Automati

Dijagram stanja



Implementacija



Verilog RTL kod

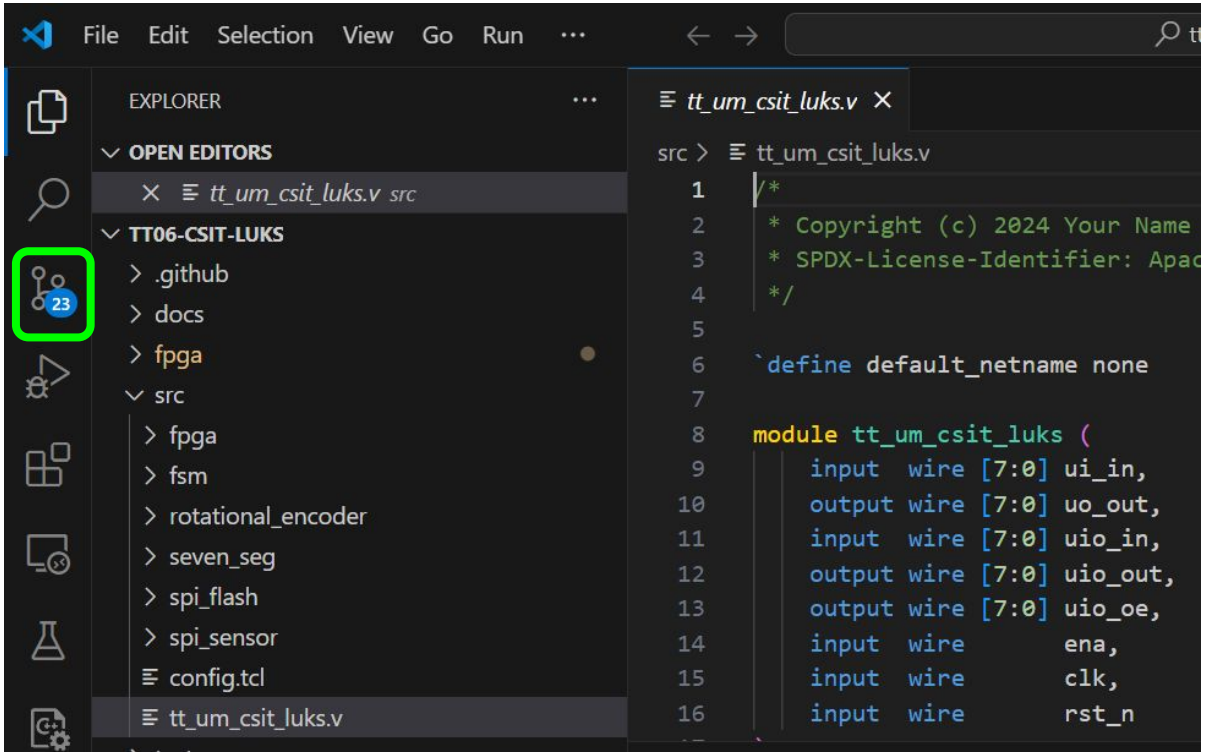
```
reg [3:0] <state> = <state1>;

always @(posedge <clock>)
   if (<reset>) begin
      <state> <= <state1>;
      <outputs> <= <initial_values>;
   end
   else
      case (state)
         <state1> : begin
            if (<condition>)
               <state> <= <next_state>;
            else if (<condition>)
               <state> <= <next_state>;
            else
               <state> <= <next_state>;
            <outputs> <= <values>;
         end
```

Rad na tt06-csit-luks

Github repozitorij

- https://github.com/jk2102/tt06-csit-luks



Ciljevi

- Definicija spojne liste (portlist)
- Testbench pojedinih modula
- Testbench top level wrappera
- FPGA prototip